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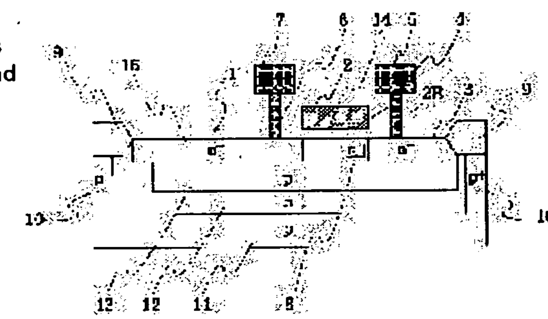
(54) PHOTOELECTRIC TRANSDUCER AND MANUFACTURING METHOD THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To form the embedded region of a photoelectric transducer, using a threshold modulation-type MOS transistor with satisfactory reproducibility and to provide a pixel and a chip, whose characteristics are adjusted.
SOLUTION: The transducer has a photodiode and an insulation gate-type transistor; the embedded region 8 of high impurity concentration for collecting charges generated in the photodiode is arranged, in a well 13 below the gate electrode of the transistor; and the embedded region 8 is self-matched with the source side end part of the gate electrode 2.



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CLAIMS

[Claim(s)]
[Claim 1] the transistor of a photodiode and an insulated-gate mold -- having -- the well of the gate electrode lower part of said transistor -- in order to collect the charges generated with said photodiode inside -- this -- a well and the said **** type -- it is -- this -- the photo-electric-conversion equipment characterized by adjusting said embedding field at the edge of said gate electrode of said transistor in the photo-electric-conversion equipment with which the embedding field of high high impurity concentration was prepared from the well.
[Claim 2] Said embedding field is photo-electric-conversion equipment according to claim 1 which is in said channel field side from the low high-impurity-concentration field which is directly under said gate electrode of said transistor, and constitutes the source field of said transistor.
[Claim 3] the transistor of a photodiode and an insulated-gate mold -- having -- the well of the gate electrode lower part of said transistor -- inside In the manufacture approach of photo-electric-conversion equipment that the embedding field of high high impurity concentration was prepared from the well in order to collect the charges generated with said photodiode -- this -- a well and the said **** type -- it is -- this -- So that the edge of said gate electrode of said transistor may be made to adjust the process which forms a 1st **** type well in a semi-conductor base, the process which forms said gate electrode of said transistor, and said embedding field said well -- the manufacture approach of the photo-electric-conversion equipment characterized by including the process which performs ion implantation inside.
[Claim 4] Said embedding field is photo-electric-conversion equipment according to claim 1 with which it is formed of slanting ion implantation after forming said gate electrode of said transistor, and said a part of embedding field [at least] is located directly under said gate electrode.

[Claim 5] The source field of said transistor is the manufacture approach of the photo-electric-conversion equipment according to claim 3 which forms by performing the ion implantation of an opposite **** type dopant so that the dopant driven in that said embedding field should be formed may be negated.
[Claim 6] The manufacture approach of the photo-electric-conversion equipment according to claim 3 which performs the ion implantation for forming said embedding field, forms the side spacer of the gate electrode of said MOS transistor, and forms the high high-impurity-concentration field of the source field of said MOS transistor after that after forming said gate electrode of said transistor.
[Claim 7] The manufacture approach of the photo-electric-conversion equipment according to claim 3 formed by rotation ion implantation so that the source field of said transistor may be surrounded for said embedding field after forming said gate electrode of said transistor.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the photo-electric-conversion equipment used for image pick-up equipments, such as a digital still camera, a video camera recorder, facsimile, and an image scanner, and the manufacture approach, and a twist concrete target at the MOS mold photo-electric-conversion equipment and its manufacture approach of a threshold modulation mold.
[0002]
[Description of the Prior Art] Need is increasing quickly as that to which photo-electric-conversion equipment fitted the image pick-up equipment for 1-dimensional image reading consisting mainly of a digital still camera, the image pick-up equipment for a two-dimensional image input centering on a video camera recorder or facsimile, and a scanner in recent years.
[0003] The photo-electric-conversion equipment of CCD (Charge Coupled Device: charge-coupled device) or an MOS mold is used as these photo-electric-conversion equipments. Since [that sensibility is high] the noise is small, while it has spread as high-definition image pick-up equipment as compared with the latter, power

consumption is large, since the former cannot use the general-purpose semi-conductor manufacture process that driver voltage is high, its cost is high and it is difficult to accumulate circumference circuits, such as a drive circuit.

[0004] Therefore, it can be expected that many the so-called MOS type of photo-electric-conversion equipments which used the transistor of an insulated-gate mold are applied to application to the pocket device by which expansion of need will be expected from now on. In order to improve the lowness of the image quality which was the fault of MOS mold photo-electric-conversion equipment for that purpose, component structure which can control a noise by the smaller transistor count is desired.

[0005] Since there are few transistor counts per pixel, BCMD (Bulk Charge Modulated Device) is devised more in ancient times as photo-electric-conversion equipment with which a numerical aperture also with a detailed big pixel is obtained.

[0006] The technique of detecting a charge can be considered by bringing together the charge generated with the photodiode as an advanced type of BCMD in the high concentration impurity layer embedded directly under the channel of an MOS transistor, and changing the threshold of an MOS transistor with a charge.

[0007] Drawing 14 - drawing 17 are drawings for this invention person to explain advanced BCMD invented previously, and drawing 14 is a sectional view according [accord / the 1-pixel circuit diagram and drawing 15 / the top view / drawing 16 R> 6] to the AA' line of drawing 15 .

[0008] The high-concentration embedding field in which the charge which generated the contact which the contact field which the gate electrode of the MOS transistor by which a threshold modulation is carried out with the photodiode which carries out photo electric conversion of the light which carried out incidence of 1, and the charge which generates 2 from a photodiode 1, and 3 connect a source field with the source field of an MOS transistor and connects 4 with wiring, and 5 connect the drain field of an MOS transistor with a source electrode, and connects 6 with wiring, and 7 with a drain electrode, and generated 8 with a photodiode 1 brings together, and 9 are component isolation regions.

[0009] and the channel stop field 10 and a well -- in p-type silicon, the source field 16, and the drain field 15, a field 13 consists of n mold silicon. a well -- a field 13 is formed in n mold field 12, and n mold field 12 is on p mold substrate 11. the embedding field 8 -- a well -- the same **** type as a field 12 -- a well -- it consists of high-concentration p-type silicon from a field 12.

[0010] a photodiode 2 -- a well -- the well which is the configuration that a part of field 13 serves as an anode, and a part of drain field 15 and n mold field 12 serve as a cathode

and by which the hole was made the suspension condition among the charges generated by the light which carried out incidence there -- it is accumulated in a field 13, and is collected and accumulated in the embedding field 8 where potential is low for a hole.
[0011] Here, with reference to drawing 17 , signs that the conductivity of an MOS transistor is modulated with this stored charge are explained. Drawing 17 expands and shows the gate electrode and the structure of a lower part of an MOS transistor. The hole 21 generated with the photodiode is accumulated in the embedding field 8. This charge generates the mirror image charge 22 to the gate electrode 2. The threshold of the MOS transistor part of mirror image charge 22 directly under changes with these mirror image charges 22. In the operating state by which the fixed gate voltage for read-out is impressed to the gate electrode 2, the current which flows between the source drains of an MOS transistor will change with these operations according to a threshold.
[0012] Next, the manufacture approach of the photo-electric-conversion equipment shown in drawing 15 and drawing 16 is explained. Epitaxial growth is performed to p-type silicon 11, and n type layer 12 is formed. Next, the whole is oxidized thinly, then a silicon nitride is deposited, and etching removal of the oxide film / the silicon nitride of a component isolation region is carried out. After carrying out the ion implantation of the p mold ion and forming the channel stop field 10 between pixels, LOCOS oxidation is performed and the component isolation region 9 is formed. regist patterning -- forming -- this -- a mask -- carrying out -- ion -- devoting oneself -- a well -- a field 13 is formed. Next, the resist pattern for forming an embedding field is formed, and the ion implantation which made this the mask is performed. Next, after forming gate dielectric film 14 in a front face, polish recon is deposited and patterning is carried out to a gate electrode configuration. The source field 16 of n mold and the drain field 15 are formed by the ion implantation by using this gate electrode 2 as a mask. Then, deposition of an insulator layer, opening of contact, deposition of a wiring metal membrane, and patterning are performed, and contacts 4 and 6 and the source drain electrodes 5 and 6 are formed.
[0013]
[Problem(s) to be Solved by the Invention] However, since it varies for every lot of the wafer at the time of every chip of the photo-electric-conversion equipment which the distance to the embedding field 8 and the source field 16 of an MOS transistor manufactures, and manufacture, the sensibility of photo-electric-conversion equipment will differ in the above-mentioned manufacture approach. The reason is for the relative position of the embedding field 8 and the source field 16 to influence sensibility as it is

explained below. Variation deltaVth of the threshold of an MOS transistor is :deltaVth=Q/C expressed as follows. -- (formula 1)
However, like drawing 17 , the electrostatic capacity and also C which are formed between the charge 21 with which Q is stored in an embedding field and the amount C of savings **** charges is stored in an embedding field, and its mirror image charge 22 are embedded from under an insulator layer 14, and serve as the capacity Cg of the gate dielectric film 14 of the MOS transistor of the right above of the embedding field 8 from the series capacitance of the electrostatic capacity Csi of the silicon field to a field 8. Therefore, C=Cg-Csi/(Cg+Csi) -- (formula 2)
Since it is proportional to a charge transform coefficient, i.e., the output voltage generated with one generating charge, the detection sensitivity which is the important property of photo-electric-conversion equipment is eta=e/C. -- (formula 3)
However, eta is a capacity as which a charge transform coefficient and e are defined by elementary charge, and C is defined by (the formula 2).
[0014] The rate which carries out termination into the source field among the line of electric force which comes out of a charge 21 as the embedding field 8 approaches the source field 16, although termination of the line of electric force 23 which comes out of the charge 21 which embeds like [the distance to the gate electrode 2 from the embedding field 8 embeds, and / when sufficiently shorter than the distance to the source electrode from a field] drawing 17 , and is stored in a field is altogether carried out to the mirror image charge 22 in a gate electrode becomes large. Therefore, the mirror image charges by which induction is carried out into a gate electrode decrease in number that much. It becomes impossible therefore, for the charge which embedded and was brought together in the field to produce threshold change of an MOS transistor effectively. This means that sensibility falls.
[0015] As mentioned above, the sensibility of photo-electric-conversion equipment will vary with the distance to the embedding field 8 and the source field 16. When the distance of an embedding field and a source field is taken enough, the dimension of an MOS transistor becomes large and it becomes impossible to realize detailed pixel structure.
[0016] Then, even if the purpose of this invention produces an embedding field with sufficient repeatability and makes a component dimension small, it is to suppress the heterogeneity of the sensibility for every chip and offer the manufacture approach of the photo-electric-conversion equipment which can produce the MOS transistor of the threshold modulation mold to which the property was equal in much ******.
[0017]

[Means for Solving the Problem] the 1st invention of this application -- the transistor of a photodiode and an insulated-gate mold -- having -- the well of the gate electrode lower part of said transistor -- in order to collect the charges generated with said photodiode inside -- this -- a well and the said **** type -- it is -- this -- in the photo-electric-conversion equipment with which the embedding field of high high impurity concentration was prepared from the well, said embedding field is characterized by having consistency at the edge of the gate electrode of said transistor.

[0018] The 2nd invention of this application has the transistor of a photodiode and an insulated-gate mold. In the manufacture approach of photo-electric-conversion equipment that the embedding field of high high impurity concentration was prepared from the well the well of the gate electrode lower part of said transistor -- in order to collect the charges generated with said photodiode inside -- this -- a well and the said **** type -- it is -- this -- the edge of the gate electrode of said MOS transistor is made to adjust the process which forms a 1st **** type well in a semi-conductor base, the process which forms the gate electrode of said MOS transistor, and said embedding field -- as -- said well -- it is characterized by including the process which performs ion implantation inside.

[0019]

[Embodiment of the Invention] (Operation gestalt 1) The photo-electric-conversion equipment by the operation gestalt 1 of this invention is explained with reference to drawing 1 - drawing 4 .

[0020] Drawing 1 is the sectional view for 1 pixel of photo-electric-conversion equipment. A superficial configuration and circuitry are the same as that of drawing 14 and drawing 15 .

[0021] The photodiode to which 1 can generate and accumulate a charge (here hole) by incident light, and 2 are the gate electrodes of the transistor (MOS transistor) of the insulated-gate mold for read-out which performs the channel conductivity modulation by the generating carrier. Here, a photodiode 1 is constituted in one with an MOS transistor, and is the embedding mold photodiode with which pn junction was formed of the well 13 of p mold, the drain field 15 of n mold, and n mold field 12.

[0022] A layered product with polish recon, polish recon, a metal or metal silicide etc. with which the impurity was doped can be used for this gate electrode 2. 3 is a source field which consists of a n-type semiconductor of the above-mentioned MOS transistor, and can begin to photograph the output current of the MOS transistor modulated from this source field 3. The source contact which consists of conductors with which 4 was filled up in the contact hole of a non-illustrated insulating layer, such as aluminum and

a tungsten, and 5 are source electrodes (source wiring) which consist of conductors, such as aluminum and copper. The drain contact which consists of conductors with which 6 was filled up in the contact hole of a non-illustrated insulating layer, such as aluminum and a tungsten, and 7 are connected to the power source for driving an MOS transistor with the drain electrode (drain wiring) which consists of conductors, such as aluminum and copper. 8 is an embedding field and consists of a p type semiconductor of high high impurity concentration. This embedding field 8 is adjusted in source side edge section 2E of the gate electrode 2.

[0023] 9 is the component isolation region which consists of silicon oxide etc., and has prevented the cross talk with the adjoining pixel. The well 13 is surrounded, as the channel stop field where 10 consists of a p type semiconductor of high high impurity concentration for isolation, the substrate with which 11 consists of a p type semiconductor, and 12 been fields which consist of a n-type semiconductor and become independent in them for every pixel about the well 13 which consists of a p type semiconductor. The gate dielectric film with which 14 consists of silicon oxide etc., and 15 are wiring for a signal output in the drain field and the source electrode 5 which consist of a n-type semiconductor of high high impurity concentration used as a drain.

[0024] Below, actuation of this photo-electric-conversion equipment is explained briefly.

[0025] Actuation of photo electric conversion is performed in order of reset -> are recording -> read-out, and this actuation is repeated. a reset action -- the well of p mold -- all the holes that remain in the field 13 and the embedding field 8 of p+ mold are discharged to a substrate 11. Therefore, the bias voltage for reset used as forward bias (for example, about 5-10V) is impressed to the drain electrode 7 and the gate electrode 2 of an MOS transistor to a substrate 11. Since all the holes that remain in the well 13 of p mold and the embedding field 8 of p+ mold since the depletion layer prolonged from the up-and-down pn junction interface carries out the punch-through of the field 12 of n mold and depletion-izes it at this time are breathed out by the substrate 11 and the well 13 of p mold and the embedding field 8 of p+ mold are also depletion-ized, the random noise by the thermal fluctuation of a carrier is not generated.

[0026] In the are recording actuation after reset, the bias voltage for are recording (for example, 3-5V) which can carry out the reverse bias of the photodiode 1 to the drain electrode 7 is impressed. Moreover, the channel of an MOS transistor sets the gate voltage impressed to the gate electrode 2 so that it may be in an are recording condition or a depletion condition as the electrical potential difference below the threshold of an MOS transistor (for example, -3 volts - +1 volt). In this condition, incidence of the light is carried out to a photodiode 1. An electron is sucked out by the drain field 15 and the

drain electrode 7 among the charges generated by this incident light, i.e., an electronic-hole pair, and by diffusion and the drift, a hole is embedded through a well 13 p molds, and gather in a field 8. Holes gather for all of two or more embedding fields 8 with the gestalt of this operation. Moreover, the clearance between the adjoining embedding fields 8 is small designed to extent which a hole can draw near to potential inclination from one of the embedding fields 8. In read-out actuation, the modulation of the conductivity of an MOS transistor by which induction is carried out in the hole accumulated in the embedding field 8 is read from the source electrode 5 as a current of an MOS transistor. The electrical potential difference impressed to the gate electrode 2 of an MOS transistor for read-out actuation is set up more than threshold voltage. In order to secure the linearity of the current-voltage characteristic as photo-electric-conversion equipment, gate voltage is decided that an MOS transistor operates in a pentode field.

[0027] With the gestalt of this operation, if it embeds if needed and a field 8 is divided into plurality, electrostatic capacity at the time of charge detection can be made small, and the sensibility as photo-electric-conversion equipment will improve.

[0028] As the division approach of the embedding field 8, sensibility can be efficiently raised by dividing in the channel width direction (the gate width direction) of an MOS transistor.

[0029] For the side near a photodiode 1, the charges generated by incident light are diffusion and the direction which carries out a drift among the source fields 3 of an MOS transistor. In a part without the embedding field 8, a charge will not be able to be embedded, and it will not be able to catch in a field 8, but will disappear in the source field 3 of an MOS transistor. In the side which does not have a photodiode 1 among the source fields 3, such loss cannot take place easily. The design which makes sensibility max is attained the magnitude of the embedding field 8, and by changing a consistency according to the physical relationship of a photodiode and the source field of an MOS transistor.

[0030] Next, with reference to drawing 2 - drawing 4 , the manufacture approach of the photo-electric-conversion equipment by the operation gestalt of this invention is explained.

[0031] Epitaxial growth is performed to the semi-conductor substrate 11 which consists of single crystal silicon of p mold, and n type layer 12 is formed. Since n type layer thickness determines the spectral sensitivity by the side of long wavelength, the thickness is determined according to the light which should be detected. Next, in order to form the component isolation region 9, the whole is oxidized thinly, then a silicon

nitride is deposited, and etching removes the oxide film / silicon nitride of the part which should form the component isolation region 9. In order to form the channel stop field 10 committed also as isolation, ion implantation equipment is used, the ion of a p mold impurity like boron is driven in, LOCOS oxidation is performed, and the component isolation regions 9 and 10 are produced. then, the well after applying the resist which consists of a photopolymer, exposing to a predetermined pattern and developing negatives -- it heat-treats by driving p mold impurity into the part which should form a field 13. a well -- heat treatment after the amount of ion implantation of a field 13 and ion implantation is decided that-izing can be carried out [depletion] on a desired electrical potential difference, and the saturation charge of a photodiode serves as a desired value at the time of a reset action.

[0032] Next, in order to produce a gate electrode, after forming gate dielectric film 14, a conductor like polish recon is made to deposit, patterning is performed, and the gate electrode 2 is formed. In this way, the structure shown in drawing 2 is obtained.

[0033] Next, a resist is carried out with ** and the resist of the field for embedding by patterning and forming a field is removed. The field in which, as for the field in which this resist pattern PR should form the drain field of an MOS transistor, a wrap should form drawing Nakamigi side edge section 2E of a gate electrode and a source field completely is a pattern to expose. Next, the embedding field 8 of p mold is formed by the ion implantation of boron. In view of a source side, the ion at this time performs slanting ion implantation so that ion may carry out incidence in the direction of the gate. It can embed by slanting ion implantation and a part of field 8 can be formed in the direction lower part of a vertical of the gate electrode 2 (directly under). 10 degrees - 40 degrees are suitable to the normal on the front face of a substrate as whenever [tilt-angle / of ion implantation / theta]. Moreover, let the depth of the embedding field 8 be a location deeper than the effective channel of an MOS transistor. the concentration of the embedding field 8 can accumulate a hole -- as -- a well -- although there is sufficiently high-concentration need from a field 13, since it becomes impossible to negate p mold dopant by n mold dopant not much by the ion implantation at the time of next source field 3 formation when it is devoted by high douse, it is desirable that it is 1/10 or less concentration of the concentration of the source field 3 formed behind. In this way, the structure shown in drawing 3 is obtained.

[0034] After removing a resist pattern PR, the source field 3 of n mold and the drain field 15 are formed by ion implantation and heat treatment by using a gate electrode as a mask. Rather than the time of placing of p mold dopant, the part by which a mask is not carried out with the gate electrode 2 among p+ mold fields poured in for embedding

field 8 formation adjusts the depth of ion implantation, and sets up more doses so that n+ mold may negate p+ mold. Consequently, among p+ mold fields, only the part directly under the gate remains as a p+ mold field, and serves as the embedding field 8 in which a charge is brought together. In this way, the structure shown in drawing 4 is obtained. In this way, self align of the embedding field 8 is carried out to edge 2E of the gate electrode 2. Then, deposition of an insulator layer, opening of contact, deposition of a wiring metal membrane, and patterning are repeated, and the structure as shown in drawing 1 is obtained. A non-illustrated metal protection-from-light layer is formed if needed after that. When producing the photo-electric-conversion equipment for colors, the color filter stratification and a micro lens are formed after this.

[0035] (Operation gestalt 2) Drawing 5 is the sectional view of the photo-electric-conversion equipment by this operation gestalt. Opening of contact, wiring, etc. are omitted and illustrated. This operation gestalt makes the source of an MOS transistor, and drain structure the so-called LDD (Lightly Doped Drain) structure. In order to form LDD structure, the side spacer 20 by the insulator layer is formed in the side attachment wall of the gate electrode 2.

[0036] Epitaxial growth is performed to p-type silicon 11, and n type layer 12 is formed. Next, in order to form a component isolation region, the whole is oxidized thinly, then a silicon nitride is deposited, and etching removal of the oxide film / the silicon nitride of a component isolation region is carried out. After driving in the ion of p mold dopant and forming the high-concentration channel stop field 10 between pixels, LOCOS oxidation is performed and the component isolation region 9 is formed. regist patterning and ion implantation -- a well -- a field 13 is formed. a well -- heat treatment after the ion implantation dose of a field 13 and ion implantation is decided that-izing can be carried out [depletion] on a desired electrical potential difference, and the saturation charge of a photodiode serves as a desired value at the time of a reset action. In order to determine the impurity profile of the channel of an MOS transistor, the impurity layer of p mold and n mold is formed near a channel by the ion implantation if needed. Polish recon is deposited after forming gate dielectric film 14 in a front face, and patterning of the gate electrode is carried out. Next, Resist PR is carried out with ** and the resist of the field which embeds by patterning and forms a field is removed. The wrap is exposing [the resist pattern PR] source side edge section 2E of a gate electrode, and a source field for the drain field of an MOS transistor completely. Next, the embedding field 8 of p mold is formed by the ion implantation of boron. In view of a source side, ion performs slanting ion implantation so that incidence may be aslant carried out in the direction of the gate. It can embed by slanting ion implantation and a part of field can be formed

directly under a gate electrode. 10 degrees - 40 degrees are suitable as whenever [tilt-angle / of impregnation / theta]. Moreover, let the depth of the embedding field 8 be a location deeper than the channel of an MOS transistor. the concentration of the embedding field 8 can accumulate a hole -- as -- a well -- although there is sufficiently high-concentration need from a field 13, since it becomes impossible to negate p mold dopant by n mold dopant by the ion implantation at the time of next source field formation not much when it is devoted by high douse, it is desirable that it is 1/10 or less concentration of the concentration of a source field. In this way, the structure shown in drawing 6 is obtained.

[0037] It is the same as the operation gestalt 1 mentioned above so far.

[0038] Next, the ion of Lynn is driven in and it forms, after removing Resist PR, the low high-impurity-concentration fields 15b, 16c, 16d, and 16e, i.e., the electric-field relaxation layers, of a source drain of n mold. At this time, the field which drove in Lynn among the p+ fields 8 by the ion implantation of n mold sets up the depth of p+ layer, and concentration beforehand so that p+ mold may be negated mostly. therefore, a part of field 16c by which the electric-field relaxation field of a source field will remain in a silicon front face as an n type layer soon, and embedding field -- denying -- almost -- neutrality or a well -- there are not 16d of fields of the almost same concentration as a field 13 and an embedding field, and it is divided into three fields of field 16e of the same concentration as a drain side. The embedding field 8 is formed in the bottom of a gate electrode in self align at the edge of a gate electrode. Next, after depositing silicon oxide etc. with a CVD method, it leaves silicon oxide only to the side attachment wall of the gate electrode 2 by anisotropic etching, and the so-called side spacer 20 is formed. In this way, the structure of drawing 7 is obtained.

[0039] High-concentration source field 16a of n mold and drain field 15a are formed by ion implantation by using the gate electrode 2 as a mask. As a low-concentration electric-field relaxation field remains only in the bottom of the side spacer 20 by formation of high-concentration n mold fields 15a and 16a and it was shown in drawing 5 in this way, source electric-field relaxation field 16b and drain electric-field relaxation field 15b are formed. In this way, the embedding field 8 and the source field 3 are made by source side edge section 2E of a gate electrode in self align.

[0040] Then, deposition of an insulator layer, opening of contact, deposition of a wiring metal membrane, and patterning are repeated, and a non-illustrated metal protection-from-light layer is formed in the last, and it completes. When producing the photo-electric-conversion equipment for colors, the color filter stratification and a micro lens are formed after this.

[0041] (Operation gestalt 3) Drawing 8 shows the 1-pixel top view of the photo-electric-conversion equipment with which the MOS transistor by which a threshold modulation is carried out was made into the shape of a ring. For the photodiode to which 1 generates and accumulates a charge by incident light, the gate electrode of the MOS transistor for read-out with which 2a performs the channel conductivity modulation by the generating carrier, and 2b, as for the source field of the above-mentioned MOS transistor, and 4, gate wiring and 3 are [source contact and 5] source electrodes. Gate electrode 2a encloses the source field 3 by the shape of a ring. 6 is drain contact of an MOS transistor and 7 is a drain electrode. 8 is two or more embedding fields, and in accordance with the configuration of a gate electrode, it is divided and it is arranged so that a source field may be surrounded. 9 is a component isolation region. Drawing 9 is BB' cross section of drawing 8 . As for the gate dielectric film of an MOS transistor, and 15, the well and opposite **** type field where the channel stop field of the high concentration [10] for isolation and 11 enclose a silicon substrate, and 12 encloses a well 13, and 14 are [a drain field and 16] source fields.

[0042] With this operation gestalt, gate electrode 2a is made into the shape of a ring, and in accordance with the configuration of gate electrode 2a, it is arranged so that the embedding field 8 may also surround the source field 15. Since the large gate width of an MOS transistor can be taken while the holes diffused from the photodiode can be collected certainly, making a gate electrode into the shape of a ring can drive a bigger output load. Therefore, it is effective in improvement in the speed of read-out.

[0043] Next, the manufacture approach is explained.

[0044] The process which forms a gate electrode is completely the same as the above-mentioned operation gestalten 1 and 2. That is, epitaxial growth is performed to p-type silicon 11, and n type layer 12 is formed. Next, in order to form a component isolation region, the whole is oxidized thinly, then a silicon nitride is deposited, and etching removal of the oxide film / the silicon nitride of a component isolation region is carried out. After driving in and carrying out the ion of p mold dopant and forming the high-concentration channel stop field 10 between pixels, LOCOS oxidation is performed and the component isolation region 9 is completed. regist patterning and ion implantation -- a well -- a field 13 is formed. a well -- heat treatment after the dose of the ion implantation of a field 13 and ion implantation is decided that-izing can be carried out [depletion] on a desired electrical potential difference, and the saturation charge of a photodiode serves as a desired value at the time of a reset action. In order to determine the impurity profile of the channel field of an MOS transistor, the impurity layer of p mold and n mold is formed near a channel by ion implantation if needed.

Polish recon is deposited after forming gate dielectric film 14 in a front face, and patterning of the gate electrode is carried out. In this way, the structure shown in drawing 10 is obtained. Next, the resist of the field which carries out a resist with **, embeds by patterning like the operation gestalt 1, and forms a field 8 is removed. The resist pattern PR is exposing the field where a wrap serves as source side edge section 2E of a gate electrode, and the source completely in the field used as the drain of an MOS transistor. Next, the embedding field 8 of p mold is formed by the ion implantation of boron. Ion implantation is performed by the so-called rotation ion implantation method for attaching an inclination to a silicon front face, and rotating a wafer to a normal. By this approach, to all the directions surrounding the source field 16, it can embed in the fixed location directly under a gate electrode, and a field can be formed. 10 degrees - 40 degrees are suitable as whenever [tilt-angle / of ion implantation / theta]. Moreover, let the depth of an embedding field be a location deeper than the channel of an MOS transistor. the concentration of an embedding field can accumulate a hole -- as -- a well -- although there is sufficiently high-concentration need from a field 13, since it becomes impossible to negate p mold dopant by n mold dopant by the ion implantation at the time of next source field formation not much when it pours in by high douse, it is desirable that it is 1/10 or less concentration of the concentration of a source field. In this way, the structure of drawing 11 is obtained.

[0045] After removing Resist PR, the source field 16 of n mold and the drain field 15 are formed by ion implantation by using gate electrode 2a as a mask. The part by which a mask is not carried out by gate electrode 2a among p+ mold fields poured in for embedding field formation determines the depth of ion implantation, and a dose so that n+ mold may negate p+ mold. Consequently, among p+ mold fields, only the part directly under the gate remains as a p+ mold field, and serves as an embedding field in which a charge is brought together. In this way, the structure shown in drawing 12 is obtained. Self align of the embedding field 8 is carried out to the inside edge of a ring-like gate electrode in this way source side edge section 2E of a gate electrode, and here. Then, deposition of an insulator layer, opening of contact, deposition of a wiring metal membrane, and patterning are repeated, and a non-illustrated metal protection-from-light layer is formed in the last, and it completes. When producing the photo-electric-conversion equipment for colors, the color filter stratification and a micro lens are formed after this.

[0046] Moreover, it is also possible to make the source drain of an MOS transistor into LDD structure. In that case, it is possible to manufacture by the same approach as the approach shown in the operation gestalt 2.

[0047] According to each operation gestalt, since the embedding field has consistency in the gate electrode, the threshold modulation mold photo-electric-conversion equipment whose controllability of dispersion in sensibility improved can be obtained. Each of dimension dispersion of the embedding field which was the detailed big factor of sensibility dispersion, and location dispersion becomes possible [offering the photo-electric-conversion equipment of high sensitivity with small dispersion], without raising a manufacturing cost by self-align formation to the edge of the source mold of a gate electrode, since it can control simple.

[0048] Moreover, this invention acts effectively also with the photo-electric-conversion equipment which does not use a micro lens, or the monochrome photo-electric-conversion equipment which does not use a color filter.

[0049] Drawing 13 is the typical block diagram of image pick-up equipment like the digital camera which adopted the photo-electric-conversion equipment of this invention.

[0050] As for image formation optical system [like a lens] whose 31 is, the photo-electric-conversion equipment of each gestalt which 32 mentioned above, and 33, a control circuit and 34 are memory. The image of a photographic subject is exposed by the pixel of photo-electric-conversion equipment 32 through the image formation optical system 31, and changes to an electrical signal. A suitable image processing is performed by the controller and the electrical signal of the obtained image is accumulated in memory.

[0051]

[Effect of the Invention] According to this invention, the relative position of an embedding field and a gate electrode can be produced with sufficient repeatability, and the MOS transistor of the threshold modulation mold to which the property was equal in ****** of a chip or a large number can be produced.

[0052] In this way, when the property of the MOS mold photo-electric-conversion equipment of the threshold modulation mold suitable for a detailed pixel improves, it becomes possible to expand application of a pocket device, a digital camera, etc.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view of the threshold modulation mold

photo-electric-conversion equipment concerning the operation gestalt 1 of this invention.

[Drawing 2] It is a sectional view for explaining the production process of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 1 of this invention.

[Drawing 3] It is a sectional view for explaining the production process of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 1 of this invention.

[Drawing 4] It is a sectional view for explaining the production process of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 1 of this invention.

[Drawing 5] It is the sectional view of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 2 of this invention.

[Drawing 6] It is a sectional view for explaining the production process of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 2 of this invention.

[Drawing 7] It is a sectional view for explaining the production process of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 2 of this invention.

[Drawing 8] It is the sectional view of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 3 of this invention.

[Drawing 9] It is a sectional view for explaining the production process of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 3 of this invention.

[Drawing 10] It is a sectional view for explaining the production process of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 3 of this invention.

[Drawing 11] It is a sectional view for explaining the production process of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 3 of this invention.

[Drawing 12] It is a sectional view for explaining the production process of the threshold modulation mold photo-electric-conversion equipment concerning the operation gestalt 3 of this invention.

[Drawing 13] It is the mimetic diagram of the image pick-up equipment using the threshold modulation mold photo-electric-conversion equipment of this invention.

[Drawing 14] It is pixel circuitry of threshold modulation mold photo-electric-conversion equipment.

[Drawing 15] It is the pixel top view of threshold modulation mold photo-electric-conversion equipment.
[Drawing 16] It is the pixel sectional view of threshold modulation mold photo-electric-conversion equipment.
[Drawing 17] It is the partial enlarged drawing of the pixel cross section of threshold modulation mold photo-electric-conversion equipment.
[Description of Notations]
1 Photodiode
2 2a Gate electrode of an MOS transistor
3 16 Source field of an MOS transistor
4 Source Contact
5 Source Electrode
6 Drain Contact
7 Drain Electrode
8 Embedding Field
9 Component Isolation Region
13 Well -- Field
14 MOS Transistor Gate Dielectric Film
15 Drain Field

[Translation done.]